REMARKS

This is in response to the Office Action dated August 22, 2007. Claim 1 has been canceled. Claims 2-17 are now pending.

Allowable Subject Matter

Applicant notes with appreciation the Examiner's indication that claims 8-15 contain allowable subject matter. In this respect, allowable claims 8, 12 and 14 have been rewritten in independent form. Thus, claims 8-15 are now in condition for allowance given the Examiner's indication of allowable subject matter.

Applicant also notes with appreciation the Examiner's indication that the rejection based on alleged APA will be withdrawn if the specification is amended to be consistent with the priority document which was incorporated by reference in the application (see the Office Action at page 3). In this respect, the background section of the instant specification has been amended to be consistent with that of the priority document which was incorporated by reference into the instant application. Thus, the APA rejection should be withdrawn, given that the alleged APA is not prior art as explained in the filing of June 5, 2007.

Claim 2

Claim 2 stands rejected under Section 103(a) as being allegedly unpatentable over Kubota in view of Kazunari. This Section 103(a) rejection is respectfully traversed. Claim 2 has been amended to require that "the first and second signals are signals related to each other which could cause timing discrepancy problems when routed through different wires." In certain example embodiments of this invention, the first and second signals are signals related to each other which could cause timing discrepancy problems as they are routed through different wires,

for example clock signals for two or more systems (e.g., see pg. 8, lines 10+ of the instant application as filed).

In Fig. 26 of Kubota, the data signal line driver circuit SD1 is fed with a start pulse signal SST, a clock signal SCK (clock), and a select signal SCS1. SCS1 is supplied only to the data signal line driver circuit SD1, while SST and SCK are supplied to the data signal line driver circuit SD2 (see "other circuit" in claim 2) as well as the driver circuit SD1. SST/SCK and SCS1 have no timing discrepancy problems attributable to different routing. Thus, SST/SCK and SCS1 do not have the same relationship as the relationship between the first and second signals of claim 2. SCS1 is an operation control signal with which to select a circuit to be controlled from the two data signal line driver circuits SD1 and SD2. SCS1 is ON when a circuit is selected and OFF when the circuit is deselected (alternatively, OFF when the circuit is selected and ON when the circuit is deselected). Thus, SCS1 and SST/SCK raise no problems at all if time discrepancy occurs due to different routing; and claim 2 defines over the cited art in this respect.

The issues attributed to the routing of signals through different wires having different loads, for example, sampling timing discrepancy of video signals (see pages 5-6) do not exist in Fig. 26 of Kubota, and the reference is unrelated to the invention of claim 2 in this respect. Citation to Kazunari cannot overcome Kubota's flaws in this respect.

It is respectfully requested that all rejections be withdrawn. All claims are in condition for allowance.

Respectfully submitted,

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